IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : H. S. YANG, et al.

Group Art Unit: 2812

Appln. No. : 10/707,842

Examiner: W. L. Lindsay Jr.

Filed : January 16, 2004

For : METHOD AND APPARATUS TO INCREASE STRAIN EFFECT IN A TRANSISTOR CHANNEL

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, and supplemental to the Information Disclosure Statement filed on August 30, 2005, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application.

Further to the U.S. Patent and Trademark Office's decision to waive the requirement under 37 C.F.R. § 1.98 (a)(2)(i), copies of the U.S. patents and U.S. published patent applications are not enclosed herewith. However, if any copies are needed, the Examiner is respectfully requested to contact the undersigned. Copies of non-US patent documents as well as the documents listed in the "Other Documents" section of the attached PTO-1449 are enclosed.

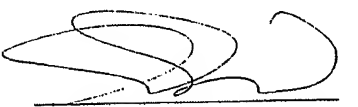
Applicants respectfully request that the Examiner consider the materials cited and indicate such consideration by appropriately initialing the enclosed PTO-1449 Form and including a copy of the initialed form in the next official communication.

Applicants note that this Information Disclosure Statement is being after receipt of a first action on the merits from the U.S. Patent and Trademark Office. Accordingly, please charge the required fee of $180.00 to **IBM Deposit Account No. 09-0458** (Fishkill).

Should the US Patent & Trademark Office conclude that other fees are required, authorization is hereby given to charge to **IBM Deposit Account No. 09-0458** (Fishkill) any fee necessary to ensure consideration of these materials.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the below listed telephone number.

Respectfully submitted,
H. S. YANG, et al.



Andrew M. Calderon
Reg. No. 38,093

May 15, 2006
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. FIS920030238	Application No. 10/707,842
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant Haining S.YANG, et al..	
	Filing Date 01/16/2004	Group 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2002/0063292 A1	5-30-2002	Armstrong et al.			
		US 2003/0032261 A1	2-13-2003	Yeh et al.			
		US 2003/0040158 A1	2-27-2003	Saitoh			
		US 2004/0238914 A1	12-2-2004	Deshpande et al.			
		US 2004/0262784 A1	12-30-2004	Doris et al.			
		US 2005/0040460 A1	2-24-2005	Chidambarrao et al.			
		US 2005/0082634 A1	4-21-2005	Doris et al.			
		US 2005/0093030 A1	5-5-2005	Doris et al.			
		US 2005/0098829 A1	5-12-2005	Doris et al.			
		US 2005/0106799 A1	5-19-2005	Doris et al.			
		US 2005/0145954 A1	7-7-2005	Zhu et al.			
		US 2005/0148146 A1	7-7-2005	Doris et al.			
		US 2005/0194699 A1	9-8-2005	Belyansky et al.			
		US 2005/0236668 A1	10-27-2005	Zhu et al.			
		US 2005/0245017 A1	11-3-2005	Belyansky et al.			
		US 2005/0280051 A1	12-22-2005	Chidambarrao et al.			
		US 2005/0282325 A1	12-22-2005	Belyansky et al.			
		US 2006/0027868 A1	2-9-2006	Doris et al.			
		US 2006/0057787 A1	3-16-2006	Doris et al.			
		US 2006/0060925 A1	3-23-2006	Doris et al.			
		6,483,171	11-19-2002	Forbes et al.			
		6,831,292	12-14-2004	Currie et al.			
		6,717,216	4-6-2004	Doris et al.			
		6,825,529	11-30-2004	Chidambarrao et al.			
		7,015,082	3-21-2006	Doris et al.			
		6,974,981	12-13-2005	Chidambarrao et al.			
		6,977,194	12-20-2005	Belyansky et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		JP 64-76755	3-22-1989	Japan				X

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. FIS920030238	Application No. 10/707,842
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant Haining S.YANG, et al..	
	Filing Date 01/16/2004	Group 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		G. Zhang, et al., "A New 'Mixed-Mode' Reliability Degradation Mechanism in Advanced SI and SiGe Bipolar Transistors." IEEE Transactions on Electron Devices, vol. 49, no. 12, December 2002, pp. 2151-56.
		H.S. Momose, et al., "Temperature Dependence of Emitter-Base Reverse Stress Degradation and its Mechanism Analyzed by MOS Structures." 1989 IEEE, Paper 6.2, pp. 140-143.
		C.J. Huang, et al., "Temperature Dependence and Post-Stress Recovery of Hot Electron Degradation Effects in Bipolar Transistors." IEEE 1991, Bipolar Circuits and Technology Meeting 7.5, pp. 170-173.
		S.R. Sheng, et al., "Degradation and Recovery of SiGe HBTs Following Radiation and Hot-Carrier Stressing," pp. 14-15.
		Z. Yang, et al., "Avalanche Current Induced Hot Carrier Degradation in 200 GHz SiGe Heterojunction Bipolar Transistors." pp. 1-5.
		H. Li, et al., "Design of W-Band VCOs with High Output Power for Potential Application in 77 GHz Automotive Radar Systems." 2003, IEEE GaAs Digest, pp. 263-66.
		H. Wurzer, et al., "Annealing of Degraded non-Transistors-Mechanisms and Modeling." IEEE Transactions on Electron Devices, vol. 41, no. 4, April 1994, pp. 533-38.
		B. Doyle, et al., "Recovery of Hot-Carrier Damage in Reoxidized Nitrided Oxide MOSFETs." IEEE Electron Device Letters, vol. 13, no. 1, January 1992, pp. 38-40
		H.S. Momose, et al. "Analysis of the Temperature Dependence of Hot-Carrier-Induced Degradation in Bipolar Transistors for Bi-CMOS." IEEE Transactions on Electron Devices, vol. 41, no. 6, June 1994, pp. 978-987.
		M. Khater, et al., "SiGe HBT Technology with Fmax/Ft = 350/300 GHz and Gate Delay Below 3.3 ps". 2004 IEEE, 4 pages.
		J.C. Bean, et al., "GEx SI 1-x/Si Strained-Layer Superlattice Grown by Molecular Beam Epitaxy". J. Vac. Sci. Technol. A 2(2), Apr.-June 1984, pp. 436-440.
		J.H. Van Der Merwe, "Regular Articles". Journal of Applied Physics, Volume 34, No. 1, January 1963, pp. 117-122.
		J.W. Matthews, et al., "Defects in Epitaxial Multilayers". Journal of Crystal Growth 27 (1974), pp. 118-125.
		Subramanian S. Iyer, et al. " Heterojuction Bipolar Transistors Using Si-Ge Alloys". IEEE Transactions on Electron Devices, Vol. 36, No. 10, October 1989, pp. 2043-2064
		R.H.M. Van De Leur, et al., "Critical Thickness for Pseudomorphic Growth of Si/Ge Alloys and Superlattices". J. Appl. Phys. 64 (6), 15 September 1988, pp. 3043-3050
		D.C. Houghton, et al., "Equilibrium Critical Thickness for SI 1-x GEx Strained Layers on (100) Si". Appl. Phys. Lett. 56 (5), 29 January 1990, pp. 460-462
		Q. Quyang et al., "Two-Dimensional Bandgap Engineering in a Novel Si/SiGe pMOSFET with Enhanced Device Performance and Scalability". 2000, IEEE, pp. 151-154.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.